A novel, aerosol-nanocrystal floating-gate device for non-volatile memory applications

J. De Blauwe, M. Ostraat*, M. L. Green, G. Weber, T. Sorsch, A. Kerber, F. Klemens, R. Cirelli, E. Ferry, J. L. Grazul, F. Baumann, Y. Kim, W. Mansfield, J. Bude, J. T. C. Lee, S. J. Hillenius, R. C. Flagan*, and H. A. Atwater*

Lucent Technologies, 600 Mountain Ave., Murray Hill, NJ 07974
*California Institute of Technology, 1200 E. California Blvd., Pasadena, CA 91125
deblauwe@lucent.com

Abstract

This paper describes the fabrication, and structural and electrical characterization of a new, aerosol-nanocrystal floating-gate FET, aimed at non-volatile memory (NVM) applications. This aerosol-nanocrystal NVM device features program/erase characteristics comparable to conventional stacked gate NVM devices, excellent endurance (>10^5 P/E cycles), and long-term non-volatility in spite of a thin bottom oxide (55-60Å). In addition, a very simple fabrication process makes this aerosol-nanocrystal NVM device a potential candidate for low cost NVM applications.

Introduction

The memory operation of the aerosol-nanocrystal floating-gate FET depends on charge storage, similar to conventional stacked-gate NVM devices [1]. In a nanocrystal NVM device, however, charge is not stored on a continuous floating-gate poly-Si layer, but instead on a layer of discrete, crystalline Si-nanocrystals [2-4]. As compared to conventional stacked-gate NVM devices, nanocrystal charge-storage offers several potential advantages such as: (1) simple, low cost device fabrication (no dual-poly process complications); (2) better retention (resulting from Coulomb blockade and quantum confinement effects [5]), enabling thinner tunnel oxides and lower operating voltages; (3) improved anti-punchthrough performance (due to the absence of drain to floating gate coupling, thereby reducing drain induced punchthrough), allowing higher drain voltages during read-out, shorter channel lengths and, consequently, a smaller cell area; and (4) excellent immunity to stress induced leakage current (SILC) and defects due to the distributed nature of the charge storage in the nanocrystal layer.

Device Fabrication

Nanocrystal layer fabrication

This potential for cost reduction and improved device performance and reliability is, however, strongly dependent on the physical properties of the nanocrystal layer, such as the crystal size and size distribution, crystal areal density, layer co-planarity and uniformity, and crystal-to-crystal interaction (lateral conduction). In order to achieve the desired layer properties, a novel, three-step nanocrystal fabrication process has been developed (Fig.1).

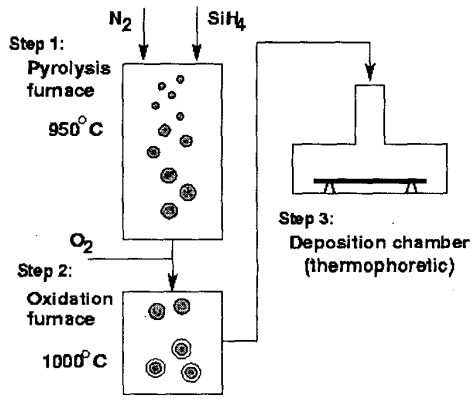

Fig. 1: Schematic representation of the aerosol fabrication process: (1) pyrolysis reaction chamber; (2) oxidation furnace; and (3) thermopherotic deposition chamber.

In the first step, a nanocrystal silicon aerosol is generated by the pyrolysis of diluted silane at 950°C. Particles initially form by homogeneous gas-phase nucleation and grow by vapor deposition and coagulation. The coagulation has been reduced by quenching the aerosol with an ultrahigh-purity nitrogen flow. Silane concentration, furnace temperature and silane residence time have all been optimized in order to generate an aerosol of spherical, single crystalline nanocrystals (Fig. 2, inset) with well-controlled diameters (Fig. 3) as small as 3nm.

In the second step, a 1.5-2nm high-quality thermal oxide shell is grown at 1000°C on the particles. This insulating shell reduces lateral crystal-to-crystal conduction in the nanocrystal layer. The oxidation step has the additional advantage of sharpening the

0-7803-6438-4/00/$10.00 ©2000 IEEE

particle size distribution since the oxidation rate decreases with decreasing nanocrystal size [6]. Finally, in the third step, a layer of nanocrystals with particle densities as high as 10^{13} cm^{-2} is thermophoretically deposited on an 8" wafer. A temperature gradient of 200°C has been used.

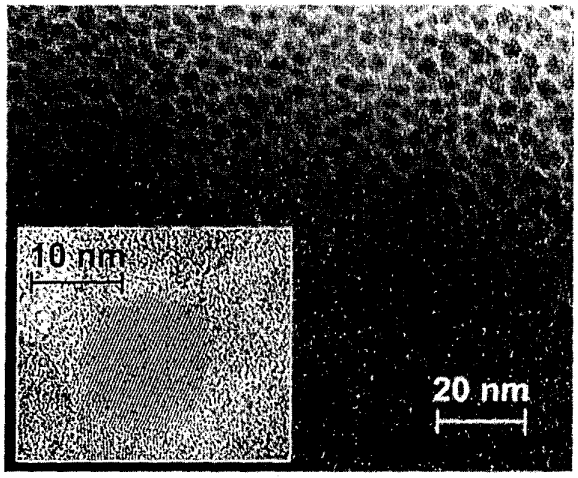

Fig. 2: Planar view of an aerosol nanocrystal monolayer. In this sample, the crystal size is 4-5nm and particle density is $6x10^{12}$. The crystallinity and spherical shape of the nanocrystals can be seen in the inset (from a different sample with 13nm particles). Tight size control and good areal coverage have been obtained.

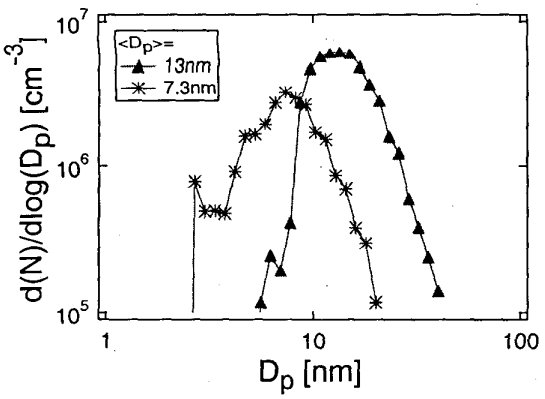

Fig. 3: Size distribution of two different aerosols, one with an average nanocrystal particle diameter of 7.3nm, the other with an average diameter of 13nm.

The aerosol technique has resulted in nanocrystal layers with a tight control over crystal morphology and a good areal coverage, as is illustrated by the planar TEM shown in Fig. 2.

NVM device fabrication

This novel nanocrystal fabrication technique has been used to integrate aerosol nanocrystal layers in 0.2μm nMOS transistors. A mono-layer of (oxidized) nanocrystals is deposited on top of a 4nm thermally grown 'tunnel' oxide, and covered with a 8nm chemical vapor deposited high temperature oxide, prior to poly-Si gate deposition.

A high-resolution cross-sectional TEM image illustrates nanocrystals incorporated in the gate dielectric stack (Fig. 4). Due to the random orientation of the deposited aerosol crystals, only about 10% of the particles can be imaged in a phase contrast image (diffraction will only occur if the lattice orientation is within 5° of the excited zone axis). The tunnel oxide thickness measured on the image is approximately 5.5nm, i.e. the sum of thicknesses of the thermal bottom oxide and the oxide shell grown on the aerosol nanocrystals prior to their deposition. Notice finally that because of the conformal nature of the HTO deposition, this image can not be used to measure the total thickness of the gate dielectric stack.

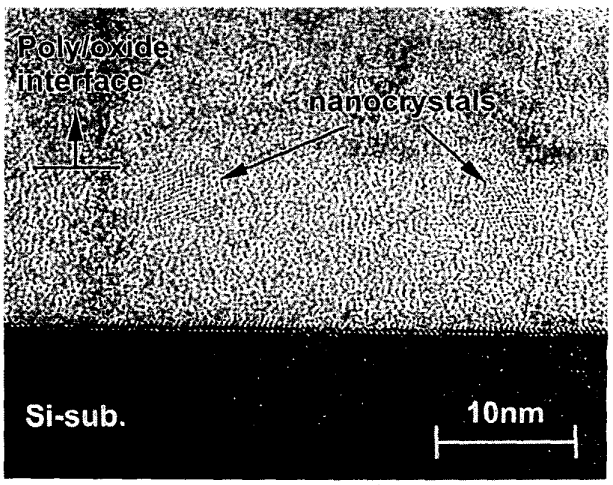

Fig. 4: Cross-sectional TEM of a nanocrystal floating-gate device, showing the tunnel oxide, the nanocrystal layer, and the high temperature top oxide. In this device, the as grown tunnel oxide and the HTO layer have a thickness of 4nm and 8nm, respectively.

Electrical Results

Typical output and subthreshold characteristics of the aerosol-nanocrystal MOSFETs are shown in Figs. 5 and 6. The values of the drive current (30μA/μm), the substrate slope (200mV/dec), and the DIBL (100mV/V) are typical for thick gate dielectric, high substrate doped NVM devices. The threshold voltage, V_t, has been defined as the gate voltage corresponding to a drain-source current of 1μA when a drain bias of 1V is applied.

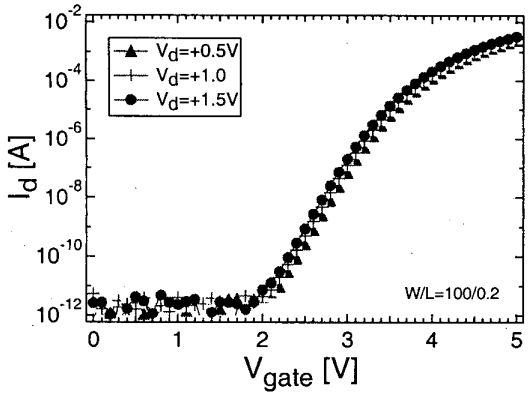

Fig. 5: Subthreshold characteristics of a 0.2μm n-type aerosol-nanocrystal floating-gate MOSFET (subthreshold slope = 200mV/dec; DIBL = 100mV/V).

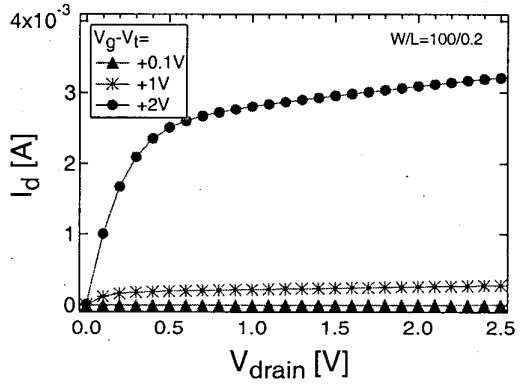

Fig. 6: Output characteristics of a 0.2μm aerosol-nanocrystal floating-gate MOSFET; drive current = 30μA/μm.

Uniform Fowler-Nordheim tunneling has been used for both the program and the erase operation, though programming using channel hot-electron injection is possible as well. As is shown in Figs. 7 and 8, the high areal nanocrystal-density obtained by the aerosol fabrication process results in a large threshold voltage window (>2V), larger than those previously reported on nanocrystal devices [4,7]. This large V_t window results in a high read-out current (20μA/μm for gate and drain biases of 2.5V and 1V, respectively), allowing fast memory access. The transient characteristics further illustrate the possible voltage/performance trade-off for this device, and show that in spite of the low gate coupling ratio (inherent to nanocrystal memories) microsecond programming and millisecond erasure is possible at moderate operating voltages.

Further, the aerosol NVM devices feature excellent endurance behavior, as is demonstrated by the small window closure observed after $5x10^5$ program/erase

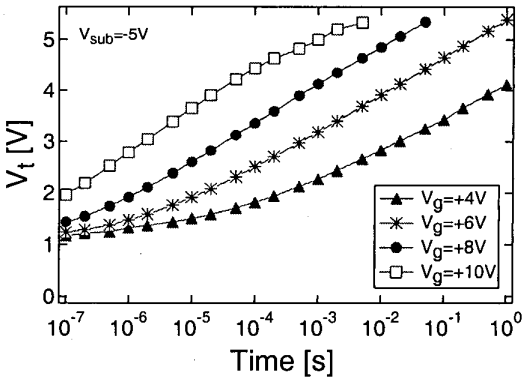

Fig. 7: Programming transients (uniform FN tunneling) of the nanocrystal NVM device. The device programs to a high V_t of +3.3V in 50μs with gate and substrate bias of +8V and –5V, respectively.

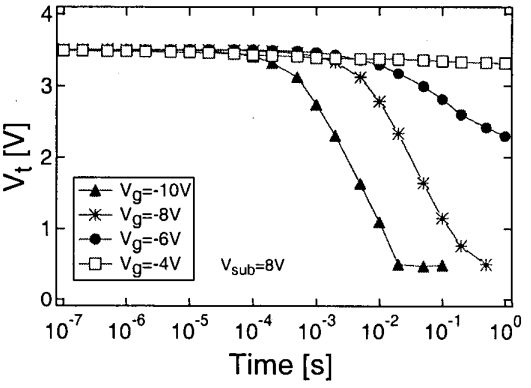

Fig. 8: Erase transients (uniform FN tunneling). The device erases to a low V_t of +1V in 100ms with gate and substrate bias of +7V and –8V, respectively.

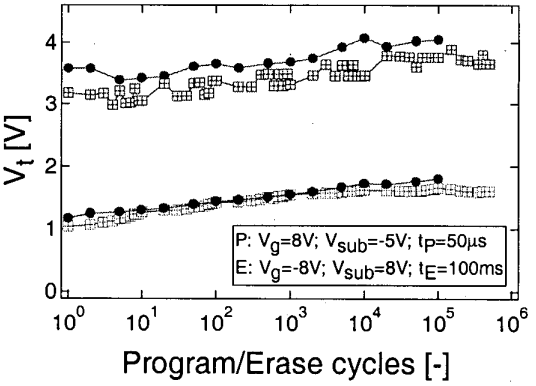

Fig. 9: Endurance characteristic; only limited window closure is observed after 10^5 program/erase cycles.

cycles (Fig. 9). The gradual shift of the V_t window to higher threshold voltages is indicative of charge being built-up in the gate oxide layer during the cycling experiment.

Disturb and retention data before and after cycling are presented in Figs. 10 and 11, and Fig. 12, respectively. In spite of the thin tunnel oxide, reasonable disturb times and long non-volatility is obtained, indicative of the intrinsic advantages of nanocrystal charge storage. Further optimization of the gate dielectric stack is necessary, though, in order to claim true non-volatility. No SILC has been observed. In addition, no drain disturb was detected, even at drain voltages as high as 4V, which indicates that there is no or only limited lateral conduction in the nanocrystal layer (Fig. 10).

Conclusions

A novel, nanocrystal floating-gate NVM device has been fabricated that is characterized by a simple, low cost fabrication process. A new, aerosol-based technique has been used to integrate a very dense (10^{13} cm^{-2}), co-planar, and uniform layer of non-coalescing, spherical, single-crystalline nanocrystals in the gate dielectric of 0.2μm MOSFET devices. As a result of these layer properties, the aerosol-nanocrystal MOSFET devices have been demonstrated to have very good electrical NVM characteristics, including a high read-out current, promising disturb behavior, excellent endurance, the absence of SILC, and long-term charge retention after cycling.

Acknowledgements

The authors would like to thank Dr. David Abusch-Magder, Dr. Ken Evans-Lutterodt, Dr. Marco Mastrapasqua, Dr. Mark Brongersma and Dr. Doug Bell for their helpful contributions and discussions.

References:

[1] S. Lai *et. al.* "Design of an E^2PROM memory cell less than 100 square microns using 1 micron technology" in *IEDM Tech. Dig.*, p. 468, 1984.

[2] S. Tiwari *et. al.* "Volatile and non-volatile memories in silicon with nano-crystal storage" in IEDM Tech. Digest, p. 521, 1995.

[3] K. Yano *et. al.* "Room-temperature single-electron memory" IEEE T-ED, vol. 41, p. 1628, 1994.

[4] H. Hanafi et. al. "Fast and long retention time nano-crystal memory" in IEEE T-ED, vol 43, p. 1553, 1996.

[5] S. Tiwari *et. al.* "Single charge and confinement effects in nano-crystal memories" APL **69** (9), p. 1232, 1996.

[6] R. Okada and S. Iijima. "Oxidation property of silicon small particles" APL **58** (15), p. 1662, 1991.

[7] K. Saito *et. al.* "Narrow channel MOS memory based on silicon nano-crystals", IEEE Silicon Nanoelectronics workshop, p. 17, 1998.

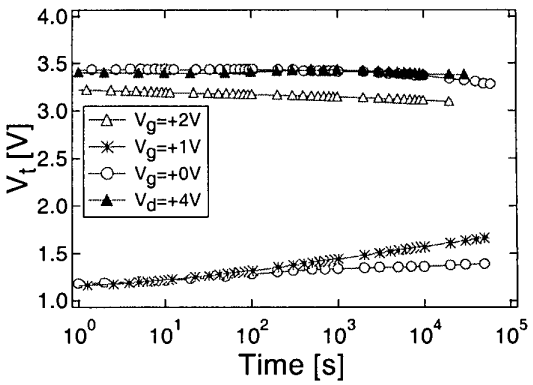

Fig. 10: Gate and drain disturb characteristics. Zero bias is applied to all nodes except for the node mentioned in the legend, i.e. either the gate (V_g) or the drain (V_d).

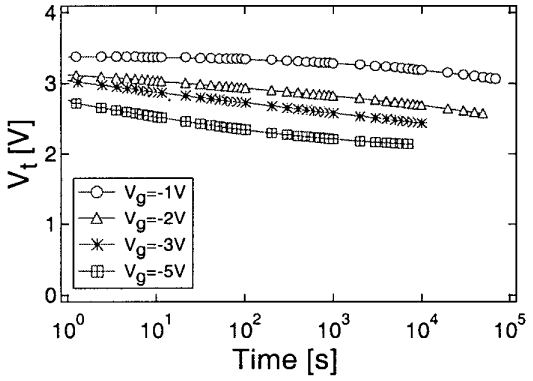

Fig. 11: Gate disturb characteristics. A negative bias is applied to the gate while all other nodes are kept grounded.

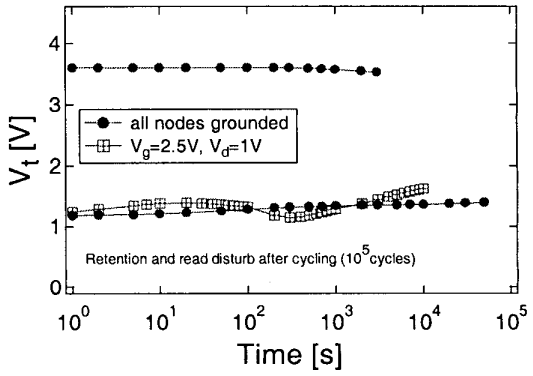

Fig. 12: After cycling, long room-temperature non-volatility is observed under both retention and read-out conditions (note: the intrinsic V_t is approximately 3V).